REMARKS

Applicants have now had an opportunity to carefully consider the Examiner's comments set forth in the Office Action of November 30, 2004.

All of the points raised by the Examiner are addressed herein. Reconsideration of the application is requested. Claims 1-21 remain in the application with this amendment.

The Office Action

Claims 1, 3, 6, 7, 10, 11, and 21 stand rejected under 35 USC § 103(a) for obviousness over U.S. Patent No. 5,995,771 to Miyawaki in view of U.S. Patent No. 4,807,259 to Yamanaka et al. (Yamanaka).

Claim 2 stands rejected under 35 USC § 103(a) for obviousness over Miyawaki in view of Yamanaka and further in view of U.S. Patent No. 6,675,249 to Shimoda et al. (Shimoda).

Claims 4 and 8 stand rejected under 35 USC § 103(a) as being unpatentable over Miyawaki in view of Yamanaka and further in view of U.S. Patent No. 6,343,351 to Lackman et al. (Lackman).

Claim 12 stands rejected under 35 USC § 103(a) as being unpatentable over Miyawaki in view of Yamanaka and further in view U.S. Patent No. 6,704,302 to Einbinder et al. (Eindbinder).

Claims 5, 9, and 13-20 stand rejected under 35 USC § 103(a) as obvious over Miyawaki in view of Yamanaka and further in view of U.S. Patent No. 5,535,217 to Cheung et al. (Cheung).

The Examiner has made the above rejections final.

The Art Rejections

Rejection of Claims 1-21 and Finality of Rejection Does Not Provide Applicants With Fair Opportunity to Identify the Issues and Reply Because Examiner Has Not Properly Communicated the Basis for Rejection.

The Examiner has rejected claims 1-21 under 35 USC § 103(a) for obviousness over various combinations of references in the Office Action of November 30, 2004 and has made these rejections final. The applicants

respectfully request reconsideration of the finality of these rejections because: i) the Examiner has not properly communicated the basis for rejection of the claims so that the issues can be identified as required by MPEP § 706.02(j), ii) the Examiner has not fully and clearly stated the ground for rejection as required by MPEP § 707.07(d), and iii) the Examiner has not designated the particular parts of references that are relied upon for rejection of each claim individually as required by 37 CFR 1.104(c).

For example, according to paragraph 6 of the Office Action the Examiner has rejected independent claim 21 under 35 USC § 103(a) for obviousness over Miyawaki in view of Yamanaka. Then, at paragraph 13, the Office Action refers to findings 4.2, 4.9, and 4.10 as to rejection of claim 21. Paragraph 4 includes paragraphs 4.1-4.41 which are fact findings for support of all rejections in the Office Action. In fact findings 4.2, 4.9, and 4.10, the Examiner identifies certain items that are disclosed in Yamanaka with column, line, and drawing references. Notably, the Examiner's rejection of claim 21 for obviousness over the combination of Miyawaki and Yamanaka is not clearly tied to any specific fact findings from Miyawaki. In a telephone interview with the Examiner on December 29, 2004, the use of fact findings from Miyawaki in rejection of claim 21 was discussed with the applicants' patent counsel. The Examiner explained that any of the Miyawaki fact findings (i.e., 4.38 - 4.41) that are relevant to claim 21 are also relied upon to support rejection of the claim in addition to the Yamanka findings specifically identified in paragraph 13. The Examiner further explained that any fact findings (i.e., 4.1 through 4.41) that are relevant to any particular claim are relied upon to support rejection of that claim. The specific findings referred to by the Examiner in paragraphs 6 through 31 are not necessarily the only findings that support the rejections.

Initially, the applicants were confused as to which specific fact findings supported rejection of certain claims, particularly where rejection was based on a reference without identifying any specific fact findings associated with that reference. After the December 29 telephone interview, it is apparent that the Examiner has forced the applicants to guess which fact findings (i.e., 4.1 - 4.41) are relied upon for rejection of each claim in order to properly frame an argument to support allowance of the claim. The Examiner's Office Action does not designate the particular parts of the references relied upon for rejection of the claims and, therefore, does not provide fully and clearly stated grounds for the rejections. This

does not give the applicants a fair opportunity to reply to the rejections. Based on the foregoing, it is profoundly unfair to the applicants that the Office Action was made final. Accordingly, the applicants respectfully request reconsideration and withdrawal of the finality of the rejection of claims 1-21.

Rejection of Claims 1-21 is Improper Because Examiner Has Not Properly Established Some Suggestion or Motivation to Combine Miyawaki and Yamanaka.

The Examiner has rejected: i) claims 1, 3, 6, 7, 10, 11, and 21 under 35 USC § 103(a) for obviousness over the combination of Miyawaki and Yamanaka, ii) claim 2 under 35 USC § 103(a) for obviousness over the combination of Miyawaki, Yamanaka, and Shimoda, iii) claims 4 and 8 under 35 USC § 103(a) for obviousness over the combination of Miyawaki, Yamanaka, and Lackman, iv) claim 12 under 35 USC § 103(a) for obviousness over the combination of Miyawaki, Yamanaka, and Einbinder, and v) claims 5, 9, and 13-20 under 35 USC § 103(a) for obviousness over the combination of Miyawaki, Yamanaka, and Cheung.

The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness (MPEP § 2142). To establish a prima facie case of obviousness, inter alia, there must be some suggestion or motivation, either in the references themselves or in the art, to modify the reference or to combine reference teachings (MPEP § 2143). There are three possible sources for a motivation to combine references: i) the nature of the problem to be solved, ii) the teachings of the prior art, and iii) the knowledge of persons of ordinary skill in the art. (In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998); MPEP § 2143.01). Obviousness can be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art (MPEP § 2143.01). The Examiner has identified explicit motivation to combine Miyawaki and Yamanaka for claims 1-21 in the Office Action.

As to claim 1, the Examiner points out that Miyawaki did not discuss the details of synchronization between the controller of the marking engine and the resource (para. 7, page 8). Therefore, in order for the Examiner to establish a prima facie case of obviousness for claim 1, Yamanaka must disclose the details of

synchronization that are not discussed in Miyawaki and the Examiner must be identify a suggestion or motivation to combine the synchronization teachings of Yamanaka with the document processing system teachings of Miyawaki.

According to the Office Action, the Examiner finds explicit motivation to combine Miyawaki and Yamanaka in Yamanka and states that "one of ordinary skill in the art would have been motivated to make such a combination in order to provide a way to synchronize operations for practical use [finding 4.18]" (para. 7, page 8). Finding 4.18 states that "Yamanaka teaches the advantage of synchronizing the master and slave clocks within a range of error in order to avoid problems for practical use [col. 1, ll. 56-59]." Col. 1, lines 56-59 in the Background of the Invention section of Yamanaka states "in the time synchronization as described above, it is important that the clock circuits of the master and slave stations are synchronized within a range of error that does not result in a problem for practical use." Apparently this explicit motivation to combine Miyawaki and Yamanaka also applies to claims 2-21. During the December 29 telephone interview, the Examiner stated that Yamanaka continues to be viewed as disclosing a document processing system.

In general, Yamanaka discloses several embodiments of a data transmission and receiving system in the form of a Supervisory Control and Data Acquisition (SCADA) system that includes a master station 1 in communication with multiple remote slave stations 2, 3 (FIGs. 1, 3A, 3B, 5A, 5B). The master station serves as a control station and the slave stations provide input circuits 24, 34 and output circuits 25, 35 for two-way data transmissions to/from, for example, electrical power generating facilities, power transmission facilities, or power substation facilities of various electrical stations located within a broad region (Abstract; col. 1, lines 7-21; col. 2, lines 29-39). In this electrical station example, the master station monitors the facilities via the input circuits of the slave stations and controls the facilities via the output circuits. Various status changes of the data transmission system, such as status changes of input circuits, are detected and the time at which the status change is detected, as well as pertinent address and status information, is stored in memory (not shown) and communicated to the CPU 10 of the master station for storage, display, and printing (col. 2, line 63 – col. 3, line 31). The master clock 17 of the master station and/or the slave clocks 27, 37 of the slave stations provide the time information that is stored with status changes. As such, the master clock and

slave clocks are synchronized so that status changes across the system can be arranged in a manner that is based on the time information (col. 10, lines 31-36).

Apparently, the Examiner views the typewriter 13 and associated components of Yamanaka as a document processing system (FIGs. 1, 3A, and 5A). The CPU 10 records status changes of the slave stations 2 or 3 by operating the typewriter through the typewriter control circuit 16 (col. 3, lines 27-31). When a status change occurs, times of the slave clocks are also transmitted to the master station 1. For example, if a status change occurs at the contact being inputted to the input circuit 25 of the first slave station 2, CPU 20 transmits the time of the slave clock 27 to the master station 1 together with the address number of the relevant contact and the new status. The CPU 10 of the master station 1 stores such data to memory (not shown) and arranges the data in sequence of time added acquisition of data from other slave stations during a constant period and then outputs such data to the typewriter 13 through the typewriter control circuit 16 (col. 10, lines 24-36). Notably, neither the master nor the slave clocks synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system.

Based on the foregoing, the explicit motivation to combine Miyawaki and Yamanaka identified by the Examiner (i.e., "one of ordinary skill in the art would have been motivated to make such a combination in order to provide a way to synchronize operations for practical use") simply does not support combining any form of master/slave clock synchronization taught by Yamanaka with operation of any document processing system that may be taught by either Miyawaki or Yamanka. In particular, this does not properly provide some suggestion or motivation to combine the master/slave clock synchronization taught by Yamanaka with operations of any controller of a marking engine and an associated resource that may be taught by Miyawaki. Therefore, the applicants respectfully submit that the obviousness rejections of claims 1-21 are improper because the examiner has not properly established some suggestion or motivation to combine Miyawaki and Yamanaka. Accordingly, the applicants respectfully request that the obviousness rejections of claims 1-21 be withdrawn. Under such circumstances, the applicants respectfully submit that claims 1-21 are currently in condition for allowance.

In the Alternative, Claims 1, 3, 6, 7, 10, 11, and 21 Patentably Distinguish Over the Combination of Miyawaki and Yamanaka.

As to rejection of independent claim 1 for obviousness over the combination of Miyawaki and Yamanaka, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki) and findings 4.1-4.4 and 4.18 (Yamanaka). As to dependent claim 3, the Examiner has specifically identified finding 4.5 (Yamanaka). For dependent claim 6, the Examiner has specifically identified findings 4.6 and 4.7 (Yamanaka). As to dependent claim 7, the Examiner has specifically identified finding 4.8 (Yamanaka). For dependent claim 10, the Examiner has specifically identified finding 4.11 (Yamanaka). As to dependent claim 11, the Examiner has specifically identified finding 4.12 (Yamanaka).

In support of rejection of claim 1, the Examiner states that "Miyawaki discloses the system comprising a control bus [system bus 18], interconnecting the resource and controller [col. 4, ll. 8-11, ll. 35-39]" (finding 4.41). The applicants respectfully disagree. As shown in FIG. 2, the Miyawaki system bus 18 interconnects a CPU 11 with various other components (e.g., serial communication control unit(s) 16) within the copier controller 31 and with an interface 17 within the copier 1. Notably, the serial communication control units 16 provide the copier controller 31 with an interface to other equipment resources (e.g., operation panel, document feeder, finisher, and the like) (col. 4, lines 8-11). Therefore, the Miyawaki system bus 18 is not "interconnecting the resource and the controller" as recited in claim 1.

In further support of rejection of claim 1, the Examiner states that: i) "Yamanaka discloses a system comprising a controller, resource, and control bus with the synchronization details" (para. 7, page 8), ii) "Yamanaka discloses the system comprises a resource [slave station 2], including a slave clock [27] related to operational timing of the resource [slave station utilizes a slave clock to provide timing functionality to slave station components such as CPU 20 which inherently, requires a local timing input] and circuitry for receiving and processing the discreet clock synchronization interrupt signal [code sensing and receiving circuit 28 and CPU 20; col. 3, ll. 5-11; col. 7, ll. 12-17]" (finding 4.3) and iii) "Yamanaka discloses the system comprises a control bus [data transmission path 5], interconnecting the resource and the controller, for distribution the discrete interrupt signal [col. 2, ll. 25-28; col. 4, ll. 20-22]" (finding 4.4). The applicants respectfully disagree.

In general, Yamanaka discloses several embodiments of a data transmission and receiving system in the form of a Supervisory Control and Data Acquisition (SCADA) system that includes a master station 1 in communication with multiple remote slave stations 2, 3 (FIGs. 1, 3A, 3B, 5A, 5B). The master station serves as a control station and the slave stations provide input circuits 24, 34 and output circuits 25, 35 for two-way data transmissions to/from, for example, electrical power generating facilities, power transmission facilities, or power substation facilities of various electrical stations located within a broad region (Abstract; col. 1, lines 7-21; col. 2, lines 29-39). In this electrical station example, the master station monitors the facilities via the input circuits of the slave stations and controls the facilities via the output circuits. Various status changes of the data transmission system, such as status changes of input circuits, are detected and the time at which the status change is detected, as well as pertinent address and status information, is stored in memory (not shown) and communicated to the CPU 10 of the master station for storage, display, and printing (col. 2, line 63 – col. 3, line 31). The master clock 17 of the master station and/or the slave clocks 27, 37 of the slave stations provide the time information that is stored with status changes. As such, the master clock and slave clocks are synchronized so that status changes across the system can be arranged in a manner that is based on the time information (col. 10, lines 31-36).

Apparently, the Examiner views the typewriter 13 and associated components of Yamanaka as a document processing system (FIGs. 1, 3A, and 5A). The CPU 10 records status changes of the slave stations 2 or 3 by operating the typewriter through the typewriter control circuit 16 (col. 3, lines 27-31). When a status change occurs, times of the slave clocks are also transmitted to the master station 1. For example, if a status change occurs at the contact being inputted to the input circuit 25 of the first slave station 2, CPU 20 transmits the time of the slave clock 27 to the master station 1 together with the address number of the relevant contact and the new status. The CPU 10 of the master station 1 stores such data to memory (not shown) and arranges the data in sequence of time added acquisition of data from other slave stations during a constant period and then outputs such data to the typewriter 13 through the typewriter control circuit 16 (col. 10, lines 24-36).

Notably, neither the master nor the slave clocks synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system. Moreover, the

slave station 2 is not "a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine" as recited in claim 1. Therefore, Yamanaka does not disclose a "resource" having the characteristics alleged by the Examiner in para. 7 and finding 4.3. As such, the Yamanaka data transmission path 5 is not interconnecting "a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine" and the controller as recited in claim 1. Therefore, Yamanaka does not disclose a "control bus" having the characteristics alleged in para. 7 and finding 4.4. Accordingly, based on the foregoing, the applicants respectfully submit that claim 1 and claims dependent thereon (including claims 3, 6, 7, 10, and 11) are currently in condition for allowance on these alternative grounds.

As to rejection of independent claim 21 for obviousness over the combination of Miyawaki and Yamanaka, the Examiner has specifically identified findings 4.2, 4.9, and 4.10 (Yamanaka). In support of rejection of claim 21, the Examiner states that: i) "Yamanaka discloses the system comprises a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and logic for receiving the discrete interrupt signal [code sending and receiving circuit 28 and 38], processing the discrete interrupt signal [CPU 20 and 30], and synchronizing the slave clock with the master clock [col. 7, ll. 42-47] (finding 4.9) and ii) "Yamanaka discloses the system comprises electrical wiring [data transmission path 5] interconnecting the resources and the controller for distributing the discrete interrupt signal to the resources [col. 2, ll. 25-28; col. 4, ll. 20-22] (finding 4.10). The applicants respectfully disagree.

First, the Examiner has not specifically identified any reference that discloses or fairly suggests the "marking engine" element of claim 21. Additionally, as discussed above in the arguments that distinguish claim 1 from findings 4.3 and 4.4, neither the master nor the slave clocks in Yamanaka synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system. Moreover, the slave stations 2, 3 are not resources that are "associated with transfer of the sheet to the marking engine or receipt of the sheet from the marking engine" as recited in claim 21. Therefore, Yamanaka does not disclose a "resource" having the characteristics alleged by the Examiner in finding 4.9. As such, the Yamanaka data transmission path 5 is not interconnecting "resources associated with transfer of the

sheet to the marking engine or receipt of the sheet from the marking engine" and the controller as recited in claim 21. Accordingly, based on the foregoing, the applicants respectfully submit that claim 21 is currently in condition for allowance on these alternative grounds.

In the Alternative, Claim 2 Patentably Distinguishes Over the Combination of Miyawaki, Yamanaka, and Shimoda.

As to rejection of claim 2 for obviousness over the combination of Miyawaki, Yamanaka, and Shimoda, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.4 (Yamanaka), and 4.33 (Shimoda). The applicants respectfully disagree at least as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4. Accordingly, the applicants respectfully submit that claim 2 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Shimoda on these additional grounds.

In the Alternative, Claims 4 and 8 Patentably Distinguish Over the Combination of Miyawaki, Yamanaka, and Lackman.

As to rejection of claim 4 for obviousness over the combination of Miyawaki, Yamanaka, and Lackman, the Examiner has specifically identified findings 4.5 (Yamanaka) and 4.34 and 4.35 (Lackman). The applicants respectfully disagree at least as to finding 4.5. In finding 4.5, the Examiner states "Yamanaka discloses the resource circuitry includes a processor [CPU 20] for adjusting the slave clock to provide for compatibility with the controller [col. 7, ll. 42-47]."

As discussed above in the arguments that distinguish claim 1 from findings 4.3 and 4.4, neither the master nor the slave clocks in Yamanaka synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system. Moreover, the slave station 2 is not "a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine" as recited in claim 1. Claim 4 depends from claims 1 and 3. Therefore, Yamanaka does not disclose a "resource circuitry" having the characteristics alleged by the Examiner in finding 4.5. As such, the Yamanaka CPU 20 does not provide "compatibility between the resource and controller" as recited in claim 4. Accordingly, based on the foregoing, the applicants

respectfully submit that claim 4 is currently in condition for allowance in view of Miyawaki, Yamanaka, and Lackman on these alternative grounds.

As to rejection of claim 8 for obviousness over the combination of Miyawaki, Yamanaka, and Lackman, the Examiner has specifically identified findings 4.8 and 4.13 (Yamanaka) and 4.34 and 4.35 (Lackman). The applicants respectfully disagree at least as to findings 4.8 and 4.13. In finding 4.8, the Examiner states "Yamanaka discloses the circuitry in each resource includes a processor [CPU 20 and 30] for adjusting the slave clock associated with the resource to provide for compatibility with the controller [col. 7, ll. 42-47]." In finding 4.13, the Examiner states "Yamanaka discloses a document processing system comprising a plurality of resources [slave stations 2 and 3] [col. 7, ll. 3-5]."

As discussed above in the arguments that distinguish claim 1 from findings 4.3 and 4.4, neither the master nor the slave clocks in Yamanaka synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system. Moreover, none of the slave stations 2, 3 are "a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine" as recited in claim 1. Claim 4 depends from claims 1, 6, and 7. Therefore, Yamanaka does not disclose "circuitry in each resource" having the characteristics alleged by the Examiner in finding 4.8. As such, the CPUs 20, 30 in the Yamanaka slave stations 2, 3 do not provide "compatibility between the resource and controller" as recited in claim 8. Furthermore, Yamanaka does not disclose "resources" having the characteristics alleged in finding 4.13. Accordingly, based on the foregoing, the applicants respectfully submit that claim 8 is currently in condition for allowance in view of Miyawaki, Yamanaka, and Lackman on these alternative grounds.

In the Alternative, Claim 12 Patentably Distinguishes Over the Combination of Miyawaki, Yamanaka, and Einbinder.

As to rejection of claim 12 for obviousness over the combination of Miyawaki, Yamanaka, and Einbinder, the Examiner has specifically identified findings 4.6 and 4.7 (Yamanaka) and 4.36 (Einbinder). The applicants respectfully disagree at least as to findings 4.6 and 4.7. In finding 4.6, the Examiner states "Yamanaka discloses the system includes a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and

circuitry for receiving and processing the clock synchronization interrupt signal [code sending and receiving circuit 28 and 38, CPU 20 and 30]." In finding 4.7, the Examiner states "Yamanaka discloses the control bus [data transmission path 5], interconnects each resource with the controller thereby distributing the interrupt signal to each resource [col. 2, ll. 25-28; col. 4, ll. 20-22]."

As discussed above in the arguments that distinguish claim 1 from findings 4.3 and 4.4, neither the master nor the slave clocks in Yamanaka synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system. Moreover, neither of the slave stations 2, 3 are "a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine" as recited in claim 1. Claim 12 depends from claims 1 and 6. Therefore, Yamanaka does not disclose any "resources" having the characteristics alleged by the Examiner in finding 4.6. As such, the Yamanaka data transmission path 5 is not "interconnecting the resources and the controller" as recited in claim 12. Therefore, Yamanaka does not disclose a "control bus" having the characteristics alleged by the Examiner in finding 4.7. Accordingly, based on the foregoing, the applicants respectfully submit that claim 12 is currently in condition for allowance in view of Miyawaki, Yamanaka, and Einbinder on these alternative grounds.

In the Alternative, Claims 5 and 9 Patentably Distinguish Over the Combination of Miyawaki, Yamanaka, and Cheung.

As to rejection of claim 5 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.5 and 4.18 (Yamanaka), and 4.19 and 4.21 (Cheung). Claim 5 depends from claims 1 and 3. The applicants respectfully disagree at least: i) as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4 and ii) as to finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5. The applicants also respectfully disagree at least as to finding 4.21.

In finding 4.21, the Examiner states "Cheung discloses the compatibility between the resource and the controller is such that the slave clock is synchronized to within one clock cycle of the master clock [col. 4, ll. 37-41; set the precision

values such as Q and restrict the transmission times appropriately]." Col. 4, ll. 37-41 of Cheung reads as follows:

> "In summary, given the above sequence of messages, a single round trip according to the PCS scheme produces, for Process A, a new time $U+(V-T)/2$ plus or minus a precision of $Q+(V-T)/2$. The endpoints of this new interval, as of the present time, are $U-Q$ and $U+Q+V-T$."

This portion of Cheung does not disclose or fairly suggest that "the slave clock is synchronized to within one (1) clock cycle of the master clock" as recited in claim 5. Therefore, Cheung does not disclose clock synchronization in the manner alleged by finding 4.21. Accordingly, based on the foregoing, the applicants respectfully submit that claim 5 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

As to rejection of claim 9 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.5, 4.8, 4.13, and 4.18 (Yamanaka), and 4.19 and 4.21 (Cheung). Claim 9 depends from claims 1, 6, and 7. The applicants respectfully disagree at least: i) as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4, ii) as to finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5, iii) as to findings 4.8 and 4.13 for the same reasons provided above that distinguish claim 8 from findings 4.8 and 4.13, and iv) as to finding 4.21 for the same reasons provided above that distinguish claim 5 from finding 4.21. Accordingly, based on the foregoing, the applicants respectfully submit that claim 9 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

In the Alternative, Claims 13-20 Patentably Distinguish Over the Combination of Miyawaki, Yamanaka, and Cheung.

As to rejection of independent claim 13 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.4 and 4.13-4.17 (Yamanaka), and 4.19, 4.22-4.29, and 4.32 (Cheung). The applicants respectfully disagree at least: i) as to

findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4 and ii) as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13. The applicants also respectfully disagree at least as to findings 4.16, 4.17, and 4.24-4.29.

First, in findings 4.16 and 4.17, the Examiner states the Yamanaka discloses certain operations involving the "resource." For example, finding 4.16 states that "Yamanaka discloses the method comprising generating a discrete clock synchronization interrupt signal in the controller and distributing the discrete interrupt signal to the resource via the control bus." However, as described above in distinguishing claim 1 from findings 4.3 and 4.4, Yamanaka does not disclose or fairly suggest operation of "a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine" as recited in claim 13. Therefore, Yamanaka does not disclose a "resource" having the characteristics alleged by findings 4.16 and 4.17.

Moreover, in findings 4.24-4.29, the Examiner states the Cheung discloses certain operations involving the "resource." For example, finding 4.24 states that "Cheung discloses the method comprising sending a message from the resource to the controller via the network to request the value [time U] saved for the master clock." However, Cheung does not disclose or fairly suggest operation of "a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine" as recited in claim 13. Therefore, Cheung does not disclose a "resource" having the characteristics alleged by findings 4.24-4.29.

Furthermore, in finding 4.24, the Examiner states "Cheung discloses the method comprising sending a message from the resource to the controller via the network to request the value [time U] saved for the master clock [col. 2, ll. 66-67; col. 4, ll. 8-10]. Col. 2, lines 66-67 of Cheung reads as follows:

> "A slave node sends a synchronization request at a time
> t, according to its clock."

Col. 4, lines 7-11 of Cheung reads as follows:

> "Next, Process A sends a message (4) to Process B,
> which receives the message some time later. Process
> B then obtains a time from its local clock, of a time U,
> plus or minus a precision Q (6)."

Notably, Cheung discloses that Process B obtains a time from its local clock after it receives a message from Process A. Claim 13 recites "a) saving a value of the master clock in the controller" and "d) sending a message from the resource to the controller via the network to request the value saved for the master clock." Claim 13 is distinguished from the portion of Cheung cited by the Examiner because Process B (relating to the controller) does not save a value of its clock until after it receives the message from Process A (allegedly relating to the resource). In the claim, the value of the master clock in the controller is saved in a) and the value that was saved earlier is requested in d). Therefore, Cheung does not disclose the method alleged by finding 4.24.

Additionally, in finding 4.29, the Examiner states "Cheung discloses the method comprising adding the difference value [V-T] to the value saved for the master clock [U] to determine a synchronized value [col. 4, ll. 37-41; Q=0]. Col. 4, lines 37-41 of Cheung reads as follows:

> "In summary, given the above sequence of messages, a single round trip according to the PCS scheme produces, for Process A, a new time U+(V-T)/2 plus or minus a precision Q+(V-T)/2. The endpoints of this new time interval, as of the present time, are U-Q and U+Q+V-T."

Notably, Cheung discloses: i) subtracting a first value (T) for a slave clock from a second value (V) for the slave clock, dividing the first result by two (2), and adding the second result to a value (U) for a master clock to determine a synchronized value for the slave clock. This appears to be based on saving the master clock value (U) between the first and second slave clock values (T, V) because the delay between the master and slave clocks is averaged. In contrast, claim 13 recites "h) subtracting the first value from the second value to determine a slave clock difference value; and i) adding the difference value to the value saved for the master clock to determine a synchronized value for the slave clock and setting the slave clock to the synchronized value." Notably, Cheung teaches dividing the difference between first and second slave clock values by two (2) which is not required in the claimed method. Therefore, Cheung does not disclose the method alleged by finding 4.29.

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Accordingingly, based on the foregoing, the applicants respectfully submit that claim 13 and claims dependent thereon (i.e., claim 14) are currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

As to rejection of claim 14 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.4 and 4.13-4.17 (Yamanaka), and 4.19, 4.22-4.29, and 4.32 (Cheung). The applicants respectfully disagree at least: i) as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4, ii) as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13, iii) as to findings 4.16 and 4.17 for the same reasons provided above that distinguish claim 13 from findings 4.16 and 4.17, and iv) as to findings 4.19 and 4.24-4.29 for the same reasons provided above that distinguish claim 13 from findings 4.19 and 4.24-4.29. Accordingingly, based on the foregoing, the applicants respectfully submit that claim 14 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

As to rejection of claim 15 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.2-4.4 and 4.13-4.17 (Yamanaka) and 4.19, 4.22-4.26, 4.30, and 4.32 (Cheung). The applicants respectfully disagree at least: i) as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4, ii) as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13, iii) as to findings 4.16 and 4.17 for the same reasons provided above that distinguish claim 13 from findings 4.16 and 4.17, and iv) as to findings 4.19 and 4.24-4.26 for the same reasons provided above that distinguish claim 13 from findings 4.19 and 4.24-4.26. The applicants also respectfully disagree at least as to finding 4.30.

In finding 4.30, the Examiner states "Cheung discloses the method comprising subtracting the value saved for the slave clock [time T] from the value saved for the master clock [time U] to determine an error value between the slave clock and the master clock [U-T] and using the error value in an adjustment algorithm to adjust the slave clock to be synchronized with the master clock [col. 4,

ll. 37-41; utilize V and Q in algorithm]. Col. 4, lines 37-41 of Cheung reads as follows:

> "In summary, given the above sequence of messages, a single round trip according to the PCS scheme produces, for Process A, a new time U+(V-T)/2 plus or minus a precision Q+(V-T)/2. The endpoints of this new time interval, as of the present time, are U-Q and U+Q+V-T."

Notably, Cheung discloses: i) subtracting a first value (T) for a slave clock from a second value (V) for the slave clock, dividing the first result by two (2), and adding the second result to a value (U) for a master clock to determine a synchronized value for the slave clock. This appears to be based on saving the master clock value (U) between the first and second slave clock values (T, V) because the delay between the master and slave clocks is averaged. In contrast, claim 15 recites "g) subtracting the value saved for the slave clock from the value saved for the master clock to determine an error value between the slave clock and the master clock and using the error value in an adjustment algorithm to adjust the slave clock to be synchronized with the master clock." Notably, Cheung teaches dividing the difference between first and second slave clock values by two (2) which is not required in the claimed method. Therefore, Cheung does not disclose the method alleged by finding 4.30.

Accordingingly, based on the foregoing, the applicants respectfully submit that claim 15 and claims dependent thereon (i.e., claims 16-20) are currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

As to rejection of claim 16 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.5 and 4.18 (Yamanaka), and 4.19 and 4.21 (Cheung). The applicants respectfully disagree at least: i) as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4, ii) as to finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5, iii) as to finding 4.19 for the same reasons provided above that distinguish claim 13 from finding 4.19, and iv) as to finding 4.21 for the same reasons provided above that distinguish claim 5 from finding 4.21. Accordingingly,

based on the foregoing, the applicants respectfully submit that claim 16 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

As to rejection of claim 18 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified finding 4.31 (Cheung). The applicants respectfully disagree.

In finding 4.31, the Examiner states "Cheung discloses the method wherein the periodic interval for performing the steps [a through g in application] during steady state operation of the document processing system is about two seconds [col. 4, ll. 37-41; with Q=0 and ignoring calculation time assumed to be insignificant, focus on the more significant transmission time if that be the case so that the algorithm involving Q, V, and T would yield 2]. Col. 4, lines 37-41 of Cheung reads as follows:

> "In summary, given the above sequence of messages, a single round trip according to the PCS scheme produces, for Process A, a new time U+(V-T)/2 plus or minus a precision Q+(V-T)/2. The endpoints of this new time interval, as of the present time, are U-Q and U+Q+V-T."

Notably, Cheung discloses: i) subtracting a first value (T) for a slave clock from a second value (V) for the slave clock, dividing the first result by two (2), and adding the second result to a value (U) for a master clock to determine a synchronized value for the slave clock. This appears to be based on saving the master clock value (U) between the first and second slave clock values (T, V) because the delay between the master and slave clocks is averaged. In contrast, claim 18 recites "wherein the periodic interval for performing steps a) through g) during steady state operation of the document processing system is about two seconds." Notably, Cheung teaches dividing the difference between first and second slave clock values by two (2) which is not required in the claimed method. Therefore, Cheung does not disclose the method alleged by finding 4.31.

Accordingingly, based on the foregoing, the applicants respectfully submit that claim 18 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

As to rejection of claim 19 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.4 and 4.13-4.17 (Yamanaka), and 4.19, 4.22-4.29, and 4.32 (Cheung). The applicants respectfully disagree at least: i) as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4, ii) as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13, iii) as to findings 4.16 and 4.17 for the same reasons provided above that distinguish claim 13 from findings 4.16 and 4.17, iv) as to findings 4.19 and 4.24-4.29 for the same reasons provided above that distinguish claim 13 from findings 4.19 and 4.24-4.29, and v) as to finding 4.32 for the same reasons provided above that distinguish claim 13 from finding 4.32. Accordingingly, based on the foregoing, the applicants respectfully submit that claim 19 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

As to rejection of claim 20 for obviousness over the combination of Miyawaki, Yamanaka, and Cheung, the Examiner has specifically identified findings 4.38-4.41 (Miyawaki), 4.1-4.5, 4.8, 4.13, and 4.18 (Yamanaka), and 4.19 and 4.21 (Cheung). The applicants respectfully disagree at least: i) as to findings 4.41, 4.3, and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3, and 4.4, ii) as to finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5, iii) as to findings 4.8 and 4.13 for the same reasons provided above that distinguish claim 8 from findings 4.8 and 4.13, and iv) as to finding 4.21 for the same reasons provided above that distinguish claim 5 from finding 4.21. Accordingly, based on the foregoing, the applicants respectfully submit that claim 20 is currently in condition for allowance in view of the combination of Miyawaki, Yamanaka, and Cheung on these additional grounds.

CONCLUSION

For the reasons detailed above, it is submitted all claims remaining in the application (Claims 1-21) are now in condition for allowance. The foregoing comments do not require unnecessary additional search or examination.

No additional fee is believed to be required for this Amendment B. However, the undersigned attorney of record hereby authorizes the charging of any necessary fees, other than the issue fee, to Xerox Deposit Account No. 24-0037.

In the event the Examiner considers personal contact advantageous to the disposition of this case, he/she is hereby authorized to call Patrick R. Roche or Alan C. Brandt, at Telephone Number (216) 861-5582.

Respectfully submitted,

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28 February 2005
Date

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